

REMARKS/ARGUMENTS

Claims 1-10 are pending in the present application. Claim 1 is amended to include the recited features and claims 6 and 8 are amended to place these claims in independent form. Support for the amendments to claim 1 can be found in the specification at p. 9, ll. 13-18; and support for the amendment to claims 6 and 8 can be found in claim 1 as originally filed. Reconsideration of the claims is respectfully requested.

Applicants do not concede that the originally filed claims are not patentable over the art cited by the Examiner, as the present claim amendments and cancellations are included only to facilitate expeditious prosecution. Applicants respectfully reserve the right to pursue these and other claims in one or more continuations and/or divisional patent applications.

I. Claim Objections

The examiner objects to claim 1. This objection is respectfully traversed. The examiner states that:

Claim 1 objected to because of the following informalities: the phrase "such that a signal produced by self-timing producing circuit and detected by the self-timing signal reading circuit approximates timing behavior of the memory array." in lines 7-9 is unclear, it is unclear what is detected by the self-timing reading circuit. It appears that should be to -- such that a signal produced by self-timing producing circuit is detected by the self-timing signal reading circuit approximates timing behavior of the memory array. --. Appropriate correction is required.

Office action of April 27, 2007, p. 2 (emphasis in original).

Claim 1 as amended, which retains the objected-to language, is as follows:

1. (Currently Amended) An integrated circuit comprising:
a memory array having a first side;
a self-timing signal-producing circuit located at the first side;
a self-timing signal-reading circuit located at the first side; and
a routing path connecting the self-timing signal-producing circuit to the self-timing signal-reading circuit, wherein the routing path extends into the memory array for a sufficient length such that a signal produced by the self-timing signal-producing circuit and detected by the self-timing signal-reading circuit approximates timing behavior of the memory array, and wherein the routing path causes a self-timing row decoder to simulate an effect of having the self-timing row decoder at a boundary between a first row decoder region in the memory array and a second row decoder region in the memory array.

The objected-to phrase in claim 1 is clear. The examiner's proposed amendment would render claim 1 unclear. The objected-to phrase can be read as: "such that a signal produced by (A) and detected

by (B) approximates timing behavior of the memory array." In this case, (A) is "the self-timing signal-producing circuit" and (B) is "the self-timing signal-reading circuit." Read in this light, the objected-to phrase clearly states that the signal, produced by (A) and detected by (B), approximates timing behavior of the memory array.

In contrast, the examiner's proposed amendment would read as follows: "such that a signal produced by self-timing producing circuit is detected by the self-timing signal reading circuit approximates timing behavior of the memory array." By replacing the word "and" with the word "is" the examiner would create an indefinite sentence because the objects that "approximate" would no longer be known. For example, the examiner's proposed amendment would read as follows: "such that a signal produced by (A) is detected by (B) approximates timing behavior of the memory array," where (A) is "the self-timing signal-producing circuit" and (B) is "the self-timing signal-reading circuit." In this case, the word "approximates" is a dangling verb because the verb and the subject(s) do not agree. Accordingly, Applicants respectfully decline to implement the examiner's suggested amendment.

As shown above, the original language of the objected-to phrase is clear and proper. Accordingly, Applicants request that the objection be withdrawn.

II. 35 U.S.C. § 102: Asserted Anticipation

The examiner rejects claims 1-5 and 10 as anticipated by *Maki, Semiconductor Memory Device Having Self-Timing Circuit*, U.S. Patent 6,870,777 (March 22, 2005) (hereinafter "Maki"). This rejection is respectfully traversed.

Applicants first address the rejection of claim 1. The examiner states that:

Regarding to claims 1-5, 10, *Maki* disclose an integrated circuit comprising: a memory array having a first side; a self-timing signal producing circuit (25 and/or 27) located at the first side; a self-timing reading circuit (14) located at the first side; a routing path (see at least Figs. 2- 3) connecting the self-timing signal producing circuit to self-timing reading circuit, wherein the routing path extends into the memory array for sufficient length such that a signal produced by self-timing producing circuit is detected by the self-timing signal reading circuit approximates timing behavior of the memory array; wherein the self-timing signal producing circuit is a dummy row decoder (25); wherein the self-timing signal producing circuit is a dummy cell (27); wherein the self-timing signal reading circuit is a dummy sense amplifier (14); wherein the memory array is a segment of a large segmented memory array; wherein the routing path extends into the memory array to a point that is at some intermediate location between the first side and a second side of the memory array, such that a wire delay associated with the routing path approximates a wide delay that would be experienced on a hypothetical routing path extending from the first side to the second side. See at least Figs. 2-6, for example of Col. 4, lines 10-67; Cols. 5-6; Col. 7, lines 1-42, and the related disclosure.

Office action of April 27, 2007, pp. 3-4 (emphasis in original).

A prior art reference anticipates the claimed invention under 35 U.S.C. § 102 only if every element of a claimed invention is identically shown in that single reference, arranged as they are in the claims. *In re Bond*, 910 F.2d 831, 832, 15 U.S.P.Q.2d 1566, 1567 (Fed. Cir. 1990). All limitations of the claimed invention must be considered when determining patentability. *In re Lowry*, 32 F.3d 1579, 1582, 32 U.S.P.Q.2d 1031, 1034 (Fed. Cir. 1994). Anticipation focuses on whether a claim reads on the product or process a prior art reference discloses, not on what the reference broadly teaches. *Kalman v. Kimberly-Clark Corp.*, 713 F.2d 760, 218 U.S.P.Q. 781 (Fed. Cir. 1983). In this case, each and every feature of the presently claimed invention is not identically shown in the cited reference, arranged as they are in the claims.

Claim 1 as amended is reproduced below for convenience:

1. (Currently Amended) An integrated circuit comprising:
a memory array having a first side;
a self-timing signal-producing circuit located at the first side;
a self-timing signal-reading circuit located at the first side; and
a routing path connecting the self-timing signal-producing circuit to the self-timing signal-reading circuit, wherein the routing path extends into the memory array for a sufficient length such that a signal produced by the self-timing signal-producing circuit and detected by the self-timing signal-reading circuit approximates timing behavior of the memory array, and wherein the routing path causes a self-timing row decoder to simulate an effect of having the self-timing row decoder at a boundary between a first row decoder region in the memory array and a second row decoder region in the memory array.

Maki does not anticipate claim 1 because *Maki* does not teach the claimed feature of, "wherein the routing path extends into the memory array for a sufficient length such that a signal produced by the self-timing signal-producing circuit and detected by the self-timing signal-reading circuit approximates timing behavior of the memory array," or the claimed feature of, "wherein the routing path causes a self-timing row decoder to simulate an effect of having the self-timing row decoder at a boundary between a first row decoder region in the memory array and a second row decoder region in the memory array."

With respect to the latter feature, the examiner asserts otherwise. The examiner refers to nearly the entire detailed description of *Maki* to support the examiner's assertion. Given the length of that disclosure, Applicants request that the examiner provide specific instances in the text or figures of *Maki* where the examiner believes that this claimed feature can be found.

However, *Maki* does not teach the claimed feature of, "wherein the routing path extends into the memory array for a sufficient length such that a signal produced by the self-timing signal-producing circuit and detected by the self-timing signal-reading circuit approximates timing behavior of the memory array." Generally, *Maki* is directed to a semiconductor memory device that includes a data access path

for accessing a memory cell, a signal drive circuit which drives a signal on said data access path, a dummy path that emulates said data access path, and a dummy drive circuit which emulates the signal drive circuit. *Maki*, Abstract. The dummy path has a smaller load than said data access path and the dummy drive circuit has a smaller drive capacity than the signal drive circuit. *Id.*

Maki does not teach that the routing path extends for a sufficient length such that a signal produced by the self-timing approximates timing behavior of the memory array. *Maki* does teach the following with regard to self-timing circuits:

The signals on the dummy bit lines 34 are amplified by the buffer 35 serving as a dummy sense amplifier, and are supplied to the control circuit 11. In response, the control circuit 11 generates a sense amplifier activation signal to activate the sense amplifiers of the read-write amplifier 14. The sense amplifier activation signal serves as a timing control signal that defines timing by simulating actual memory access, thereby *Making* it possible to cancel timing deviation caused by product variation in a reliable manner.

Maki, col. 7, ll. 14-22.

Maki teaches that a control circuit generates a sense amplifier activation signal to activate sense amplifiers of the read-write amplifier. The sense amplifier activation signal serves as a timing control signal that defines timing by simulating actual memory access. However, this teaching is not the same as, "wherein the routing path extends into the memory array for a sufficient length such that a signal produced by the self-timing signal-producing circuit and detected by the self-timing signal-reading circuit approximates timing behavior of the memory array," as required by claim 1. Although the timing control signal in *Maki* defines timing by simulating memory access, the timing itself does not approximate the actual behavior of the memory array. Therefore, *Maki* does not teach this claimed feature.

Additionally, *Maki* does not teach the claimed feature of, "wherein the routing path causes a self-timing row decoder to simulate an effect of having the self-timing row decoder at a boundary between a first row decoder region in the memory array and a second row decoder region in the memory array."

Maki is simply devoid of disclosure regarding this feature of claim 1.

As shown above, *Maki* does not teach all of the features of claim 1. Therefore, under the standards of *In re Bond*, *Maki* does not anticipate claim 1. At least by virtue of the dependency of claims 2-5, *Maki* also does not anticipate claims 2-5. Accordingly, this rejection is overcome.

III. 35 U.S.C. § 103: Asserted Obviousness

The examiner rejects claims 6 and 7 as obvious over *Maki*. This rejection is respectfully traversed. The examiner states that:

With respect to claims 6-7, *Maki* discloses all the limitation as applied to claim 5 above and further comprising a second path, wherein the second routing path is

route over a second segment (17). (See at least Fig. 1). *Maki* lack an inclusion of wherein the second segment made up of memory cells that are disabled through metal programming. Providing a segment made up of memory cells that are disabled through metal programming would have been known and available in the art to allow late process programming. It would have been obvious to one having ordinary skill in art at the time of the invention to modify *Maki* accordingly in order to provide memory cells with greater flexibility for later programming process in a semiconductor memory device. NOTE: for at least Col. 9, line 3-10 of Becker (6,674,661) cited to support known position.

Office action of April 27, 2007, p. 5 (emphasis in original).

The Examiner bears the burden of establishing a *prima facie* case of obviousness based on prior art when rejecting claims under 35 U.S.C. § 103. *In re Fritch*, 972 F.2d 1260, 23 U.S.P.Q.2d 1780 (Fed. Cir. 1992). The prior art reference (or references when combined) must teach or suggest all the claim limitations. *In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974). In determining obviousness, the scope and content of the prior art are... determined; differences between the prior art and the claims at issue are... ascertained; and the level of ordinary skill in the pertinent art resolved. Against this background the obviousness or non-obviousness of the subject matter is determined. *Graham v. John Deere Co.*, 383 U.S. 1 (1966). Often, it will be necessary for a court to look to interrelated teachings of multiple patents; the effects of demands known to the design community or present in the marketplace; and the background knowledge possessed by a person having ordinary skill in the art, all in order to determine whether there was an apparent reason to combine the known elements in the fashion claimed by the patent at issue. *KSR Int'l. Co. v. Teleflex, Inc.*, No. 04-1350 (U.S. Apr. 30, 2007). Rejections on obviousness grounds cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness. *Id.* (citing *In re Kahn*, 441 F.3d 977, 988 (CA Fed. 2006)).

Applicants first address the rejection of claim 6. Claim 6, now in independent form, is as follows:

6. (Currently Amended) An integrated circuit comprising:
a memory array having a first side;
a self-timing signal-producing circuit located at the first side;
a self-timing signal-reading circuit located at the first side; and
a routing path connecting the self-timing signal-producing circuit to the self-timing signal-reading circuit, wherein the routing path extends into the memory array for a sufficient length such that a signal produced by the self-timing signal-producing circuit and detected by the self-timing signal-reading circuit approximates timing behavior of the memory array, wherein the larger segmented memory array includes a second segment, and the second segment made up of memory cells that are disabled through metal programming.

As shown above, *Maki* does not teach the claimed feature of, "wherein the routing path extends into the memory array for a sufficient length such that a signal produced by the self-timing signal-

producing circuit and detected by the self-timing signal-reading circuit approximates timing behavior of the memory array." By virtue of the lack of disclosure in *Maki* in this regard, *Maki* does not suggest this claimed feature. Accordingly, under the standards of *In re Royka*, no *prima facie* obviousness rejection has been stated against claim 6. At least by virtue of the dependence of claim 7 on claim 6, no *prima facie* obviousness rejection has been stated against claim 7.

Additionally, the examiner's assertion that, "Providing a segment made up of memory cells that are disabled through metal programming would have been known and available in the art to allow late process programming" is incorrect. For example, the specification provides that:

An additional advantage to this self-timing memory design is that it allows unused portions of a memory array to be freed up for metal routing. For example, suppose that a given ASIC (application-specific integrated circuit) design does not require the full memory capacity of an available memory array. With respect to Figure 6, one could suppose that only memory 602 was needed for the particular application. Since the self-timing circuitry all resides on the bottom half of memory array 602 (rather than the typical case of extending from the top of memory array 600 down to the bottom of memory array 602, if one considers memory arrays 600 and 602 to form one larger memory array), memory array 600 (the unused portion of the larger memory array) can be used for routing other signals without interference from self-timing signals.

Specification, p. 9, l. 28 through p. 10, l. 7 (emphasis supplied).

As shown in the specification, metal routing would *not* have been known and available in the art, as the examiner asserts, because not enough physical room would have been available for the metal routing. One of the benefits of the claimed inventions is to allow metal routing to be performed because, according to the specification, "the self-timing circuitry all resides on the bottom half of memory array 602 (*rather than the typical case of extending from the top of memory array 600 down to the bottom of memory array 602*)." Thus, the specification explicitly contradicts the examiner's assertion that providing a segment made of memory cells that are disabled through metal programming would have been "known and available" in the art.

For this reason, the examiner's asserted reason to combine the references is not based on what one of ordinary skill in the art would have known or assumed about *Maki*. Accordingly, the examiner has not provided a sufficient reason to modify *Maki* to achieve the invention of claim 6. Hence, under the standards of *KSR Int'l.*, the examiner failed to state a *prima facie* obviousness rejection against claim 6.

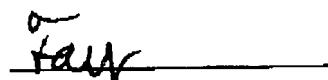
Claim 7 depends from claim 6 and therefore, at least for the above reasons, the examiner failed to state a *prima facie* obviousness rejection against claim 7. Thus, this rejection is overcome.

IV. Conclusion

The subject application is patentable over *Maki* and should now be in condition for allowance. The examiner is invited to call the undersigned at the below-listed telephone number if in the opinion of the examiner such a telephone conference would expedite or aid the prosecution and examination of this application.

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Respectfully submitted,



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